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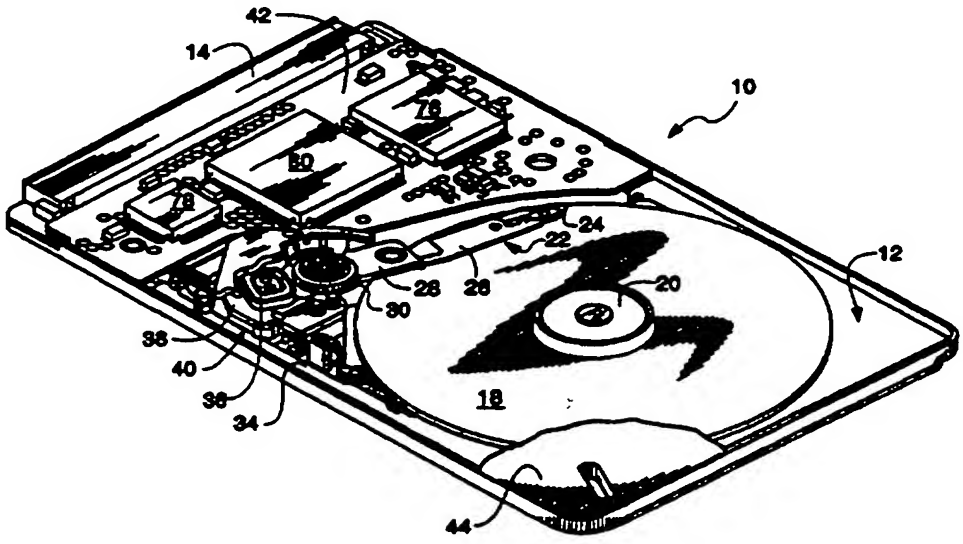

(57) Abstract

A hard disk drive (10) that latches the heads (24) of the drive away from the data sectors of the disk (18) when the drive enters an idle power down mode. Power to the voice coil motor (40) is terminated when the disk drive (10) enters the idle power down mode. Before terminating power to the voice coil motor (40), the heads (24) are moved to an inner diameter location of the disk (18) which does not contain data, commonly referred to as a landing zone. The heads (24) are maintained on the landing zone by a latch that captures a portion of the actuator arm. The latch fully secures the actuator arm (28) so that a shock load will not move the heads (24) onto the data sectors of the disk (18) and damage the same. When the disk drive (10) exits the idle power down, the latch is disengaged from the actuator arm (28), the voice coil (36) is powered up, and the heads (24) are moved back over the data sectors for subsequent disk access.

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NEW MODE FOR POWER-DOWN

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

The present invention relates to a power saving mode for a hard disk drive.

2. DESCRIPTION OF RELATED ART

Hard disk drives can draw a significant amount of power from the power supply of a computer. A large power drain can reduce the operating time of a system with a limited power supply, such as a portable computer that is running on a battery. To increase the operating time of a portable computer, schemes have been employed to "power down" various components of a disk drive when the host computer is not accessing the disk.

There are generally three different power down modes in a conventional computer. The power down modes are commonly referred to as "sleep", "standby" and "idle". If the host system has not accessed the disk within a predetermined time interval the disk drive initially enters the idle mode. In the idle mode, the voice coil motor of the actuator arm is typically turned off, but the disk is still spinning. other electronic devices such as the microprocessor may be placed into a "low" power mode to further reduce consumption of power. The disk drive may go into the idle mode either in response to a command from the host computer, or in accordance with the expiration of an

internal timer within the drive. The drive is powered back up in response to a command from the host.

In the standby mode, both the voice coil motor and the spin motor are powered down. Minimal power is provided to the disk drive host interface circuits, so that the drive can receive input commands from the host. The standby mode is typically entered after a predetermined time interval has elapsed since the last host disk access request. The standby time interval is longer than the idle time interval. Like the idle mode, the drive exits the standby mode in response to a command from the host.

The disk drive is fully powered down in the sleep mode, typically by a sleep command from the host. The drive powers up from the sleep mode when a host reset or interrupt signal is driven active. In a typical power down scenario, the disk drive will initially enter the idle mode if no host disk access command is received within a first predetermined time interval. If a host command is not received by the disk drive after the expiration of a second longer time interval, the drive will enter the standby mode. Additionally non-usage of the disk drive may cause the host to place the drive into the sleep mode.

When power to the voice coil motor is terminated, the actuator arm is typically moved to a zero spring bias position by the spring force of the flexible circuit board that is mounted to the actuator arm and electrically couples the magnetic heads to the disk electronics. The zero spring bias position is typically located above the

middle of the disk. If the drive unit is subjected to a shock load while the drive is in the idle mode, the shock load may cause the magnetic heads to strike and damage the disk. It is therefore desirable to move the heads away from the disk when the drive unit is in the idle mode.

U.S. Patent 4,933,785 issued to Morehouse discloses a disk drive which moves the heads onto a ramp when the drive enters an idle power down mode. Although the '785 drive places the heads away from the disk, the heads of the Morehouse device can still move off of the ramp and onto the disk upon the application of a shock load, particularly a shock load parallel to the plane of the disk. It would be desirable to provide a hard disk drive which fully secures the heads in a location away from the disk when the drive is in an idle power down mode.

SUMMARY OF THE INVENTION

The present invention is a hard disk drive that latches the heads of the drive away from the data sectors of the disk when the drive enters an idle power down mode. Power to the voice coil motor is terminated when the disk drive enters the idle power down mode. Before terminating power to the voice coil motor, the heads are moved to an inner diameter location of the disk which does not contain data, commonly referred to as a landing zone. The heads are maintained on the landing zone by a latch that captures a portion of the actuator arm. The latch fully secures the actuator arm so that a shock load will not move the heads

onto the data sectors of the disk and damage the same. When the disk drive exits the idle power down, the latch is disengaged from the actuator arm, the voice coil is powered up, and the heads are moved back over the data sectors for subsequent disk access.

BRIEF DESCRIPTION OF THE DRAWINGS

The objects and advantages of the present invention will become more readily apparent to those ordinarily skilled in the art after reviewing the following detailed description and accompanying drawings, wherein:

Figure 1 is a perspective view of a hard disk drive;

Figure 2 is a top sectional view of the hard disk drive;

Figure 3 is a perspective view of a latch in the unlatched position;

Figure 4 is a side view of an actuator arm in an intermediate latched position;

Figure 5 is a side view showing the actuator arm in a fully latched position;

Figure 6 is a bottom view of a printed circuit board assembly;

Figure 7 is a schematic of the system architecture of the disk drive;

Figure 8 is a schematic of a servo circuit;

Figure 9 is a schematic of a controller circuit;

Figures 10a-c are flowcharts showing the operation of the power down features of the disk drive.

DETAILED DESCRIPTION OF THE INVENTION

Referring to the drawings more particularly by reference numbers, Figure 1 shows a hard disk drive 10 of the present invention. The disk drive 10 is constructed as a card which can be plugged into a host computer (not shown). The unit 10 includes a housing 12 and a connector 14. In the preferred embodiment, the housing has a length and width of 85.6 x 54.0 millimeters, and a thickness of either 5.0 or 10.5 millimeters. The dimensions conform with the specifications issued by the Personal Computer Memory Card International Association (PCMCIA) for a type II or a type III electronic card. The PCMCIA is an association that has promulgated a specification which list dimensions and other requirements for a standard electronic card. Each computer that conforms with the PCMCIA specification will contain slots that can receive a standardized card. With such a standard, electronic cards of one computer can be readily plugged into another computer, regardless of the model or make of the systems. A copy of the PCMCIA standard can be obtained by writing to the Personal Computer Memory Card International Association at 1030 G East Duane Avenue, Sunnyvale, California 94086.

The PCMCIA standard includes three types of cards which each have varying thicknesses. A type I card is approximately 3.3 millimeters thick, a type II card is approximately 5.0 millimeters thick and a type III card is approximately 10.5 millimeters thick. The computer has a plurality of adjacent slots that are wide enough to receive

a type II card. Both the type I and II cards occupy a single slot, while the type III card occupies two slots. Each computer slot contains a 68 pin connector that is typically mounted to a motherboard to provide an interconnect to the computer system.

As shown in Figure 2, the hard disk drive contains a disk 18 that is rotated by a spin motor 20. The disk 18 rotates relative to an actuator arm assembly 22 which has a pair of transducers 24 commonly referred to as heads. The transducers 24 can magnetize and sense the magnetic field of each corresponding adjacent surface of the disk 18. Each head 24 is supported by a flexbeam 26 that is attached to an actuator arm 28. The heads 24 each contain a slider (not shown) which cooperate with the air stream produced by the rotation of the disk 18 to create an air bearing between the surface of the disk and the transducer. The air bearing lifts the head 24 off of the surface of the disk 18. The flexbeams 26 are constructed to be flexible enough to allow the heads 24 to be separated from the disk surface by the air bearings and take up the disk 18 and motor 20 axial runout.

The actuator arm 28 pivots about a bearing assembly 30 that is mounted to the base plate 34 of the disk drive. At the end of the actuator arm 28 is a voice coil 36 located adjacent to a magnet 38. The magnet and coil, commonly referred to as a voice coil motor or VCM 40, rotate the actuator arm 28 and move the heads 24 relative to the disk 18 when a current is provided to the voice coil 36. The

connector 14 is soldered to a printed circuit board 42 (PCB). The printed circuit board 42 is supported by the housing 12 and contains all of the electrical components required to operate the disk drive assembly 10. The circuit board 42, disk 18, spring motor 20 and actuator assembly 22 are all enclosed by a cover 44.

As shown in Figures 3-5, the disk drive has a latch assembly 48 that can secure the actuator arm assembly 22. The latch assembly 48 includes a block 50 mounted to the actuator arm 28. The block 50 has a slot 52 that can receive the tip 54 of a latch arm 56. Mounted to the latch arm 56 is a magnet 58 that is coupled to a latch coil 60. The latch arm 56 pivots about a pin 62 between a first position and a second position. As shown in Fig. 4, the latch arm 56 rotates to the second position when a current is provided to the latch coil 60.

To latch the actuator assembly 22, the actuator arm 28 and block 50 are moved in a counterclockwise direction to a position beyond the tip 54 of the latch arm 56. A current is then provided to the latch coil 60 to move the latch arm 54 to the second position as shown in Fig. 4. As shown in Fig. 5, the actuator arm 28 is rotated in a clockwise direction and current to the latch coil 60 is terminated to latch the arm assembly 22. The slot 52 may have a notch 64 that secures the tip 54 within the block 50. To unlatch the actuator assembly 22, the latch coil 60 is energized, the actuator arm 28 is rotated in the clockwise direction and the coil 60 is then de-energized.

As shown in Figure 6, mounted to the printed circuit board 46 is a controller chip 70, a read/write channel chip 72 and a servo chip 74. Each chip is housed within an integrated circuit package that is soldered to the board 42 by conventional techniques well known in the art. As shown in Fig. 2, the opposite side of the circuit board 42 contains a data manager chip 76, a pre-amplifier chip 78 and a read only memory (ROM) chip 80. The board 42 also contains passive elements such as resistors and capacitors to complete the electrical system of the drive assembly. The entire board 42 is located between the disk 18 and the connector 14. The electronic devices mounted to the circuit board 42 are coupled to the transducers 24, voice coil 36 and spin motor 20.

Figure 7 shows a schematic of the system architecture of the hard disk drive assembly 10. The system controls the operation of the disk drive. Data is typically stored on a magnetic disk 12 along annular tracks concentric with the diameter of the disk. Each track has a number of sectors. In the preferred embodiment, the disk is 1.8 inches in diameter. Although a 1.8 inch disk is described, it is to be understood that the present invention can be used with disks having other diameters such as 1.3", 2.5", 3.5", etc.

The system architecture includes the data manager chip 76, the controller chip 70, the servo chip 74 and the read/write ("R/W") chip 72. The system also has the read only memory ("ROM") device 80 coupled to the controller 70, and the pre-amplifier circuit ("pre-amp") 78 connected to

the heads 24 and the R/W chip 72. The controller 70 is coupled to the servo 74 and R/W 72 chips through serial lines 86 and 88, respectively. The controller 70 is coupled to the data manager 76 by address/data bus 90 and to the ROM 80 by instruction bus 92. The data manager 76 is coupled to a host system 94 by address/data bus 96 and to the R/W chip 72 by data bus 98. The R/W chip 72 is connected to the pre-amplifier chip 78 by line 100. The servo chip 74 is coupled to the R/W chip 72 through servo line 102. The servo chip 74 is also connected to the voice coil 36 and spin motor 20 through lines 104 and 106, respectively. The pre-amp chip 78 is connected to the heads 24 through line 108. The controller 70 is also coupled to the R/W chip 72 by raw data line 110. The serial lines and address/data busses contain control signal lines which are required to transfer information between the respective chips. Although the term line is used throughout this specification, it is to understood that the term line may include multiple lines.

The R/W chip 72 contains circuitry to read and write information with the disk. The data manager 76 provides an interface between the disk drive and the host 94. The manager 76 typically contains a buffer and circuitry to communicate with the host system. Instructions for performing specific disk drive functions are typically provided from the host to the drive by commands. For example, different commands are provided to read or write

data. The commands are provided to the controller 70 through the data manager 76.

As shown in Figure 8, the servo chip 60 contains a voice coil control circuit 170 and a spin motor control circuit 172 to drive the voice coil 36 and spin motor 20, respectively. The servo chip 60 is coupled to the controller chip 70 by a bi-directional 16 bit synchronous serial port 174. The serial port 174 is coupled to a digital to analog (Dac) converter 176 by lines 178. The Dac 176 contains a spin motor Dac port 180, a voice coil Dac port 182 and an analog to digital (A/D) Dac port 184.

The voice coil port 182 provides three signals Vvcmoffset, Vvcmtrack and Vcm gain range to the voice control circuit 170 on lines 188-192. The three signals are summed within a summing circuit 194. The Vvcmoffset signal provides the bias voltage for the voice coil 36. The Vvcmtrack signal provides a secondary voltage signal that will vary the bias signal to more accurately control the driving signal of the voice coil 36. The Vcm gain range signal is another secondary signal that provides a higher resolution of the bias signal and is typically employed during a servo routine of the drive. The amplitudes of the Vcm signals are determined by a 8 bit data stream which is provided by the controller chip 70 to the voice coil port 180 through the bi-directional serial port 174. The data command is accompanied by a 7 bit address and a read/write bit which are decoded by the serial port. The data is

directed to the appropriate Dac port in accordance with the contents of the 7 bit address.

The summation circuit 194 provides a signal to an operational amplifier 196 which biases a driver circuit 198. The driver circuit 198 is connected to the voice coil 36 through pins VcmP 200 and VcmN 202. The voice coil control circuit 170 also contains a current sensor 204 which is fed back to the operational amplifier 196 to provide a direct current control of the current supplied to the voice coil 36.

The spin motor port 180 provides signals Vspnoffset, Vspntrack and Vspn gain range to the spin motor control circuit 172 through lines 206-210. The signals are received by the spin motor circuit which contains essentially the same components, summation circuit 212, op-amp 214, driver circuit 216 and current sensor 218, as the voice coil circuit 170. The summing circuit 212 sums the Vspin( ) signals as described above. Like the voice coil signals, the offset signal provides a bias voltage and the other signals provide an adjustment of the bias voltage. The driver circuit 216 is connected to the windings of the spin motor through pins A, B and C on lines 220-224, respectively. The driver circuit 216 is controlled by spindle control logic 226 which sequentially enables the proper combination of drivers of the output lines A, B and C after receiving a commutation advance signal provided by the controller chip 70 on the Vcomm line 228. Each time a commutation advance signal Vcomm is provided, the control

logic 226 sequentially enables the correct drivers, so that a current is provided to the spin motor in the proper combination of lines A, B or C.

The spin motor control circuit 172 has a back emf sensor 230 connected to the lines A, B and C and the center tap (CT) of the motor on line 232. The sensor 230 provides a back emf signal to a comparator 234 which compares the signal to a reference voltage. The comparator 234 provides a Vphase signal to the controller chip 70 on line 236. The controller chip 70 utilizes the Vphase signal to commutate the spin motor 20 through the Vcomm line 228.

The voice coil control circuit 170 positions the heads 24 relative to the disk in response to commands from the controller chip 70. The controller chip 70 and control circuit 170 move the actuator pursuant to either a seek routine or a servo routine. In a seek routine the heads 24 are moved from a first track location on the disk to a second track location on the disk. The servo routine is used to maintain the transducers 24 on the centerlines of the tracks.

The servo chip also has a transistor 238 that functions as a switch for the latch coil 60. The transistor 238 is coupled to a control port 240 by line 242. The control port 240 is connected to the serial port 174. Current is provided to the latch coil 60 when the control port 240 drives line 242 active. The control port 240 is connected by line 244 to an enable circuit 246 that enables and disables the voice coil 36. Upon the receipt of a

command from the controller 70, the control port 240 can disable the enable circuit 244 so that no current is provided to the voice coil 36. Likewise, the control port 240 is coupled to the driver circuit 216 of the spin motor circuit to terminate rotation of the spin motor, through line 248. The spin motor 20 is typically braked by driving all three drive signals A, B and C active.

Figure 9 shows a schematic of the controller chip 70 which contains a core microprocessor 260. In the preferred embodiment, the core is a modified version of a processor sold by Texas Instruments Inc. ("TI") under the part designation DSP TMS320C25. The processor block 260 includes RAM memory (not shown). The DSP microprocessor has two separate internal busses (not shown) for transferring instructions and data. The dual bus architecture allows the processor to execute fetching, decoding, reading and executing routines in parallel. The pipeline feature of the DSP significantly increases the performance of the processor. The DSP processor has on board memory that functions as both registers and a RAM device.

The controller chip 70 also has supporting "on-chip" hardware coupled to the processor 260. The supporting hardware includes a bi-directional 16 bit synchronous serial port 262 that is coupled to the servo 74 and R/W chips 72 through serial lines 86 and 88. The serial port 262 contains registers that provide a buffer between the processor 260 and the chips 72 and 74. The port 262 also generates chip select signals for the R/W chip 78 and the

servo chip 74 in response to addresses provided by the processor 260. The processor 260 is coupled to the host 94 through the data manager 76 and bus 90.

The controller 70 has a state machine 268, a clock 270, an idle register 272 and a standby register 274. The clock 270 is connected to a sleep circuit 276 that is coupled to an interrupt line 278 of the host system. The sleep circuit 276 enables the clock 270 when the interrupt is driven active. The processor 260 performs operations in accordance with instructions stored in the ROM 80. The processor operations include commutating the spin motor, servo routines for the voice coil motor, transferring data between the disk and the host, and power maintenance for the disk drive. The power maintenance routine typically occurs after the spin motor and voice coil routines.

In accordance with an algorithm stored in ROM 80, if the processor 260 has not received a read or write command for a first predetermined time interval, the processor 260 will provide commands to the servo chip 74 to latch the actuator arm 28. The commands will initially move the heads 24 to an inner diameter portion of the disk. The inner diameter of the disk does not have data and is commonly referred to as a landing zone. After the heads are loaded in the landing zone, the processor 260 provides commands to latch the actuator arm 28. The processor 260 may also provide control signals to reduce power consumption in other circuits of the drive. This power down mode will be referred to as idle.

If the processor 260 has not received a read or write command for a second longer predetermined time interval, the processor 260 will generate commands for the servo chip 74 to terminate rotation of the spin motor 20. The remaining circuits except portions of the data manager 76 are also powered down. This power down mode will be referred to as standby. Alternatively, the processor 260 may generate commands to place the disk drive in the idle or standby power down modes in response to specific commands from the host 94. By way of example, the processor 260 may enter the idle mode in response to an idle command from the host. Likewise, the processor will enter the standby mode in response to a standby command from the host.

The host will typically provide idle and standby commands when the host does not access the disk within predetermined time intervals stored in corresponding registers of the host. The host may also provide a command to the processor to shut down the entire disk drive. This power down mode will he referred to as sleep. The disk drive can be "awakened" from the sleep mode by providing an interrupt signal TNT 278 to the sleep circuit 276.

The first time interval is stored in the idle register 272. The second time interval is stored in the standby register 274. The first time interval can be either set by the manufacturer or programmed through the host 94. The standby register 274 is typically programmed by the host 94. The first and second time intervals may be any value.

A zero in the idle register 272 will disable the idle mode. Likewise, a zero in the standby register 274 will disable the standby mode. The host can thereby disable the idle and/or standby mode by writing zeros in the registers 272 and 274. The processor 260 compares the values in the registers 272 and 274 with a time value computed from the last read/write command. If the time value exceeds the time intervals stored in the registers, then the processor enters the corresponding power down mode. The disk drive exists the idle and standby power down modes when the controller, receives a read/write command, or a specific command to exit the power down modes, from the host.

Figures 10a-c show a typical operation of the disk drive in the power down modes. In processing block 300, the host provides time intervals that are stored in the idle 272 and standby 274 registers. By way of example, the idle time interval may be 5 seconds and the standby time interval by be 60 seconds. The processor 260 continually compares the time from the last read/write command with the time intervals stored in the registers in decision block 302. If the time from the last read/write command exceeds the first time interval, the processor enter the idle power down mode in block 304.

In accordance with the idle power down algorithm, the processor 260 generates a set of commands that are provided to the servo chip 74 in processing block 306. The first set of commands cause the voice coil 36 to move the heads 24 into the landing zone of the disk 18. In block 308, the

processor 260 provides a set of commands to the servo chip 74, so that the control port activates the latch coil 60 to move the latch arm 56 to the second position. In block 310, the processor 260 provides a set of commands to move the actuator arm 28 into the latch block 50 and de-energizes the latch coil 60. In block 312, the processor 260 generates a set of commands to disable the voice coil 36 and possibly power down other components of the drive.

In decision block 314, the processor compares the time from the last read/write command with the second time interval stored in the standby register. If the time from the last read/write command exceeds the second time interval, then the processor 260 enters the standby power down mode in block 316. In block 318, the processor generates commands to shut down the spin motor 20 and the electronics of the drive except the data manager. The drive is maintained in the idle and/or standby modes until receiving a read/write command or a specific command from the host to exit the power down modes.

The present invention thus provides a disk drive which latches the actuator arm and maintains the heads of the drive away from the data sectors when the drive is in an idle power down mode.

While certain exemplary embodiments have been described and shown in the accompanying drawings, it is to be understood that such embodiments are merely illustrative of and not restrictive on the broad invention, and that this invention not be limited to the specific constructions

and arrangements shown and described, since various other modifications may occur to those ordinarily skilled in the art.

What is claimed is:

1. A hard disk drive that is coupled to a host computer which can provide commands, comprising:

a housing;

a spin motor mounted to said housing;

a disk attached to said spin motor, said disk having a plurality of data sectors;

an actuator arm coupled to said housing;

a transducer mounted to said actuator arm;

a voice coil coupled to said actuator arm, said voice coil receives a current to move said transducer to a non-data location away from said data sectors of said disk;

a latch that maintains said transducer at the non-data location when said voice coil moves said transducer to the non-data location; and,

an electronic circuit that controls said spin motor and said voice coil and which receives commands from the host, said electronic circuit provides current to said voice coil to move said transducer to the non-data location to engage said latch and then terminates current to said voice coil while providing current to said spin motor.

2. The hard disk drive as recited in claim 1, wherein said electronic circuit moves said transducer to the non-data location when said electronic circuit does not receive a host command for a first predetermined time interval.

3. The hard disk drive as recited in claim 1, wherein said electronic circuit moves said transducer to the non-data location in response to an idle command from the host.

4. The hard disk drive as recited in claim 2, wherein said electronic circuit spins down said spin motor when said electronic circuit does not receive a host command for a second predetermined time interval, wherein said second predetermined time interval is greater than said first predetermined time interval.

5. The hard disk drive as recited in claim 1, wherein the host provides a sleep command that terminates power to said electronic circuit.

6. The hard disk drive as recited in claim 4, wherein said first and second predetermined time intervals are stored within said electronic circuit.

7. The hard disk drive as recited in claim 2, wherein said first and second predetermined time intervals are determined by the host.

8. The hard disk drive as recited in claim 1, wherein said latch moves to a first position to allow said transducer to move to the non-data location and said latch

moves to a second position to maintain said transducer in the non-data location.

9. The hard disk drive as recited in claim 8, wherein said latch has a magnet located at an end of a lever that impedes movement of said actuator arm when said transducer is in the non-data location, said lever being coupled to a coil mounted to said housing such that a current provided to said coil moves said magnet and said lever.

10. The hard disk drive as recited in claim 1, further comprising a connector mounted to said housing and coupled to said electronic circuit, wherein said disk, said spin motor, said transducer, said actuator arm, said voice coil, said latch and said electronic circuit are all enclosed by said housing.

11. A hard disk drive that is coupled to a host computer which can provide commands, comprising:

a housing;

a spin motor mounted to said housing;

a disk attached to said spin motor, said disk having a plurality of data sectors;

an actuator arm coupled to said housing;

a transducer mounted to said actuator arm;

a voice coil coupled to said actuator arm, said voice coil receives a current to move said transducer to a non-data location away from said data sectors of said disk;

a latch that maintains said transducer at the non-data location when said voice coil moves said transducer to the non-data location; and,

an electronic circuit that controls said spin motor and said voice coil motor and which receives commands from the host, said electronic circuit provides current to said voice coil to move said transducer to the non-data location to engage said latch and then terminates current to said voice coil while providing current to said spin motor when said electronic circuit does not receive a host command for a first predetermined time interval, said electronic circuit terminates current to said spin motor when said electronic circuit does not receive a host command for a second predetermined time interval that is greater than said first predetermined time interval, said electronic circuit terminates power to said spin motor, said voice coil and said electronic circuit when said electronic circuit receives a sleep host command.

12. The hard disk drive as recited in claim 11, wherein said first and second predetermined time intervals are stored within said electronic circuit.

13. The hard disk drive as recited in claim 11, wherein said first and second predetermined time intervals are determined by the host.

14. The hard disk drive as recited in claim 11, wherein said latch moves from a first position to allow said transducer to move to the non-data location and said latch moves to a second position to maintain said transducer in the non-data location.

15. The hard disk drive as recited in claim 14, wherein said latch has a magnet located at an end of a lever that impedes movement of said actuator arm when said transducer is in the non-data location, said lever being coupled to a coil that is mounted to said housing such that a current provided to said coil moves said magnet and said lever.

16. The hard disk drive as recited in claim 11, further comprising a connector mounted to said housing and coupled to said electronic circuit, wherein said disk, said spin motor, said transducer, said actuator arm, said voice coil, said latch and said electronic circuit are enclosed by said housing.

17. A method for saving power within a hard disk drive, comprising the steps of;

a) providing a disk that is rotated by a spin motor and a voice coil that moves a transducer mounted to an actuator arm, said spin motor and said voice coil being controlled by an electronic circuit;

b) moving said transducer to a non-data location away from a plurality of data sectors of said disk;

c) latching said transducer in the non-data location; and,

d) terminating power to said voice coil while maintaining power to said spin motor.

18. The method as recited in claim 17, wherein said transducer is moved to the non-data location when a host command has not been received for a first predetermined time interval.

19. The method as recited in claim 18, further comprising the step of terminating power to said spin motor.

20. The method as recited in claim 19, wherein power to said spin motor is terminated when a host command has not been received for a second predetermined time interval that is greater than said first predetermined time interval.

21. The method as recited in claim 17, further comprising the step of terminating power to said spin motor, said voice coil motor and said electronic circuit when said electronic circuit receives a sleep host command.

22. The method as recited in claim 17, further comprising the steps of moving said latch from a first position to a second position so that said transducer can move into the non-data location, and moving said latch from the second position back to the first position to maintain said transducer in the non-data location.

23. The method as recited in claim 17, further comprising the steps of releasing said latch and moving said transducer to said data sectors of said disk in response to receiving a host command.

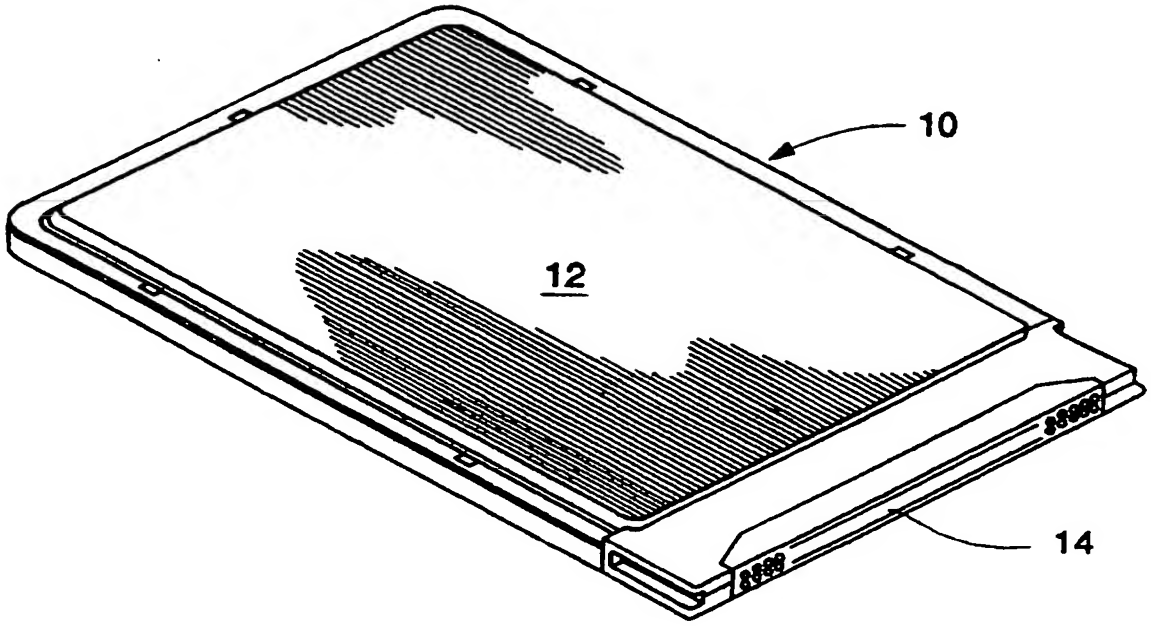

Fig. 1

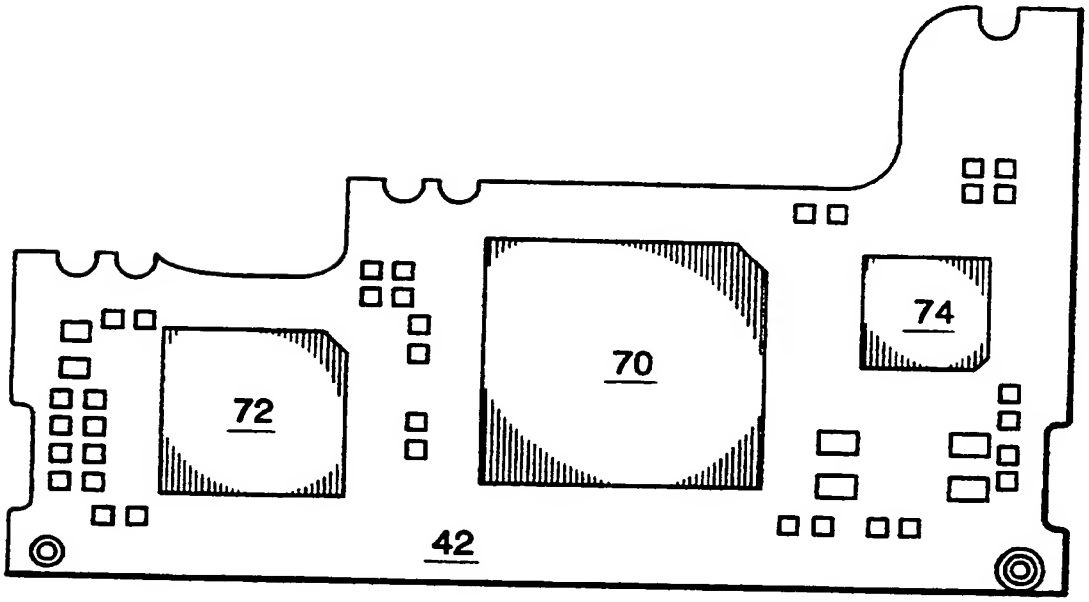

Fig. 6

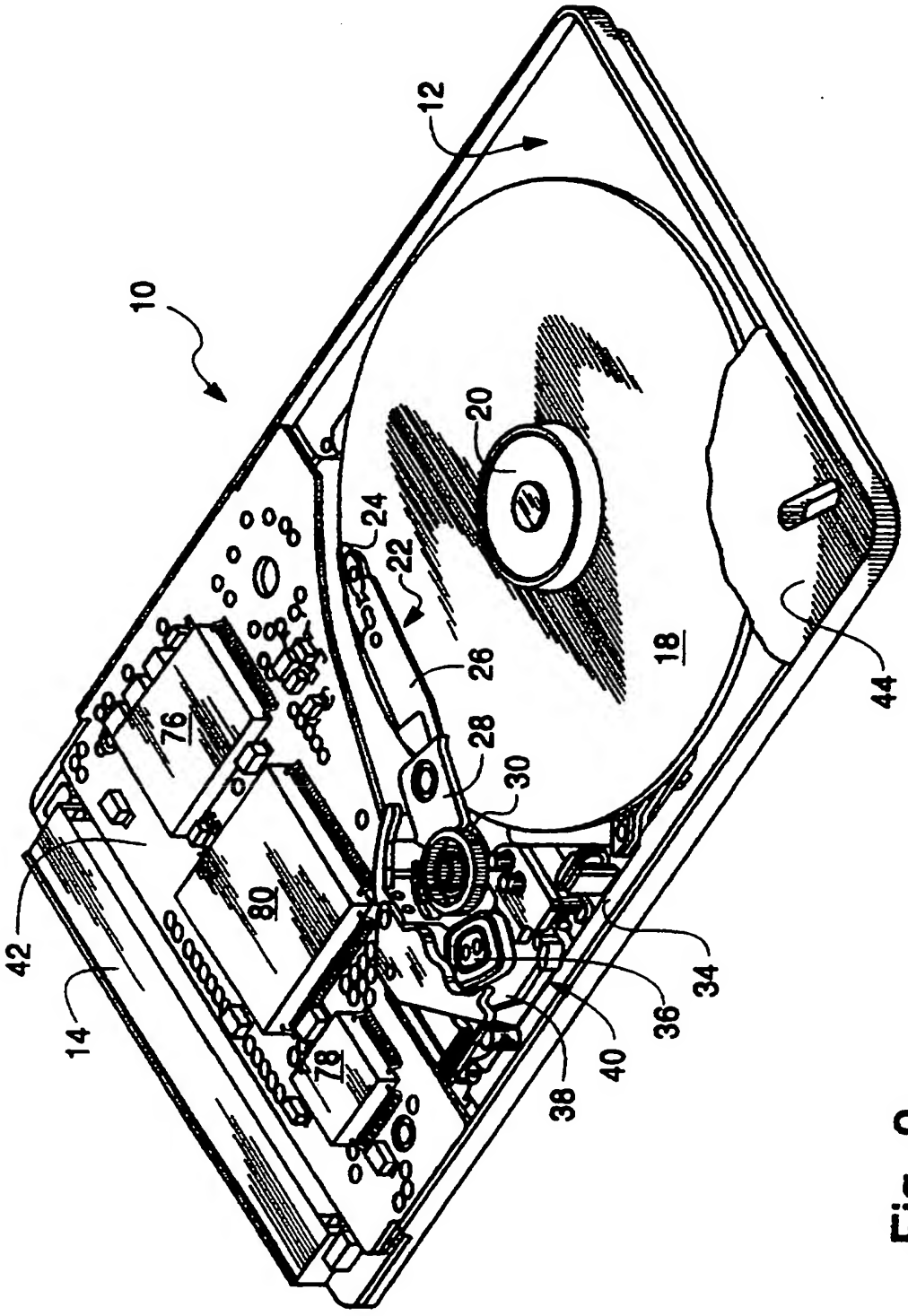

Fig. 2

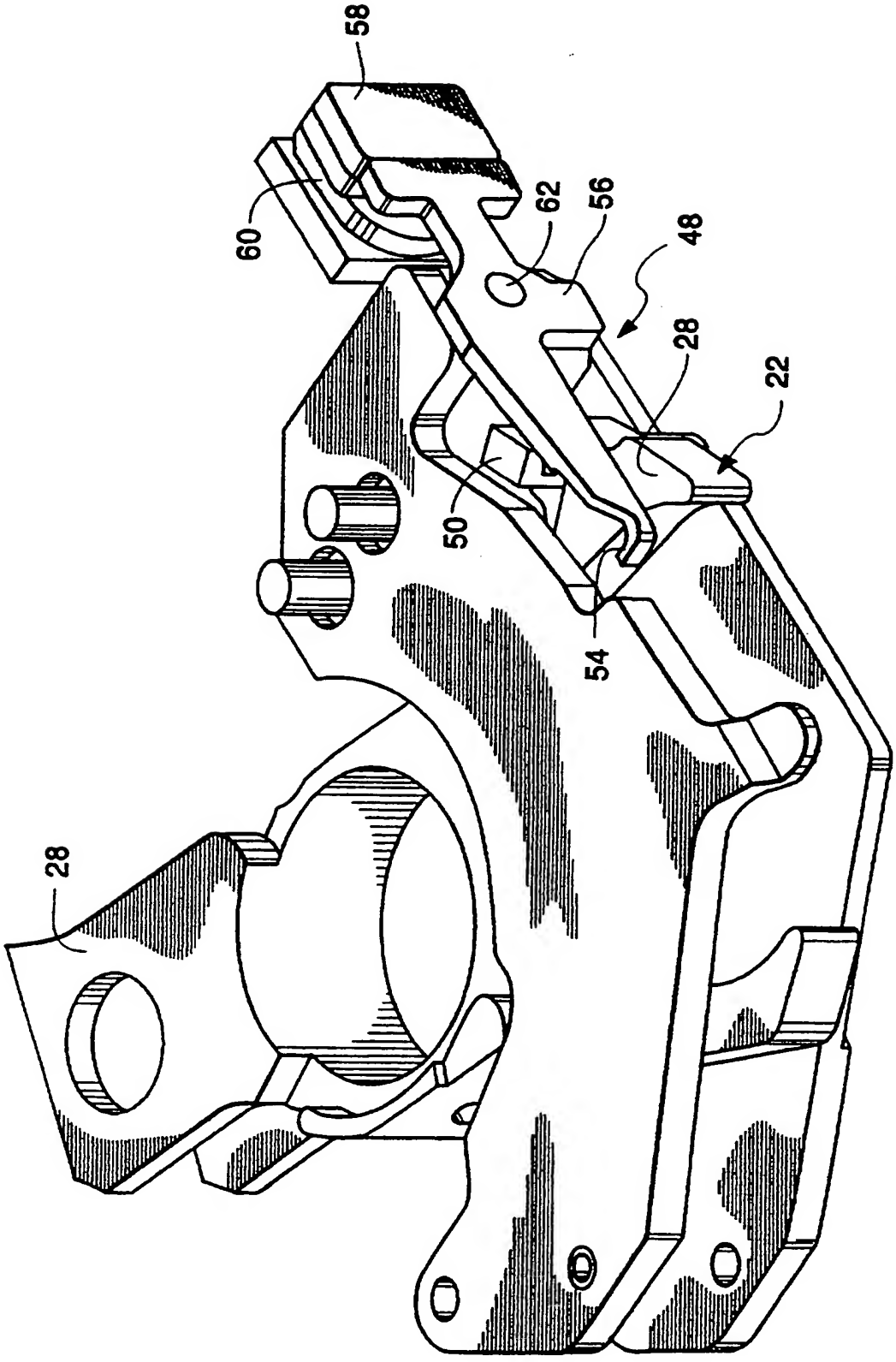

Fig. 3

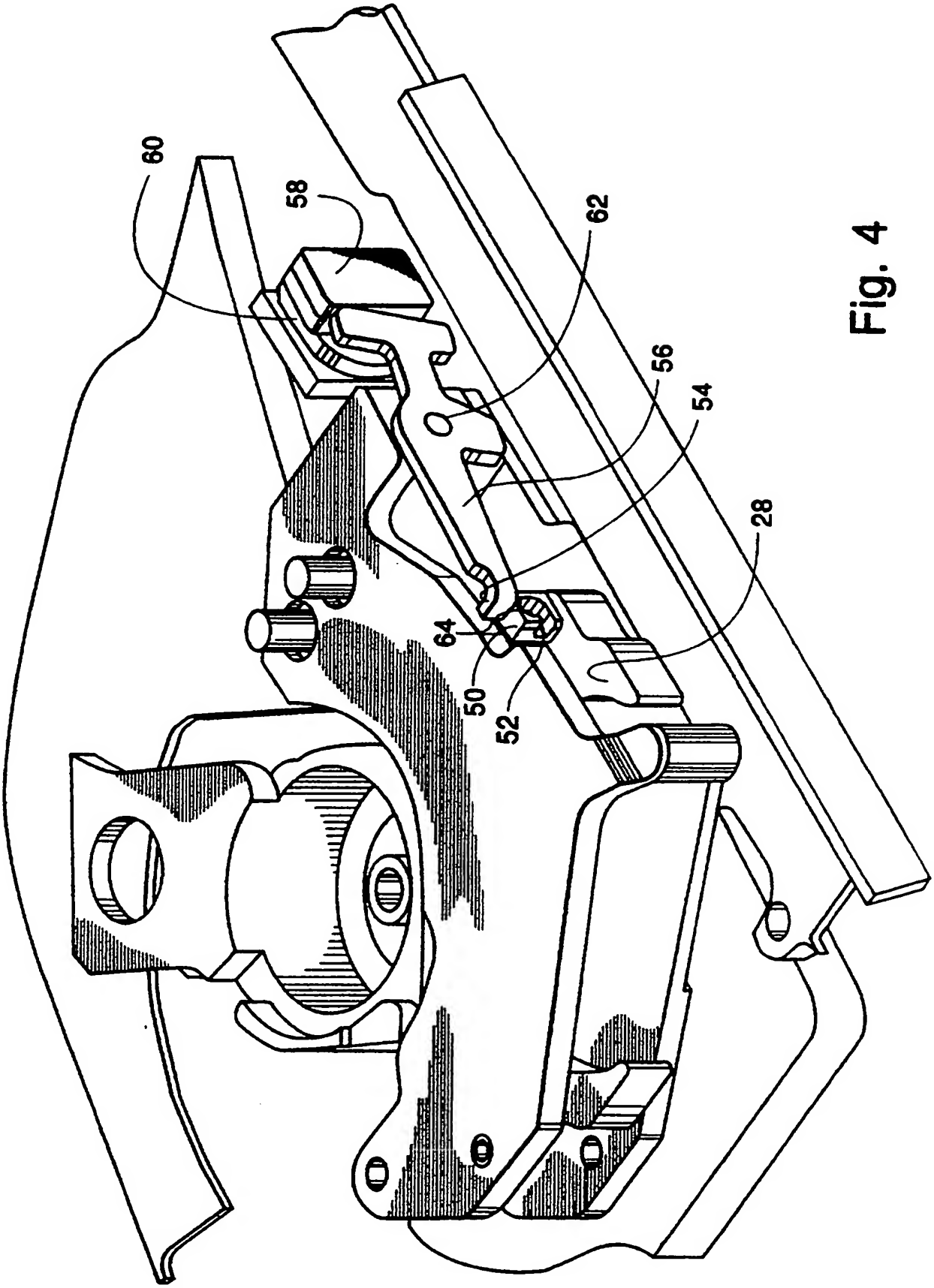

Fig. 4

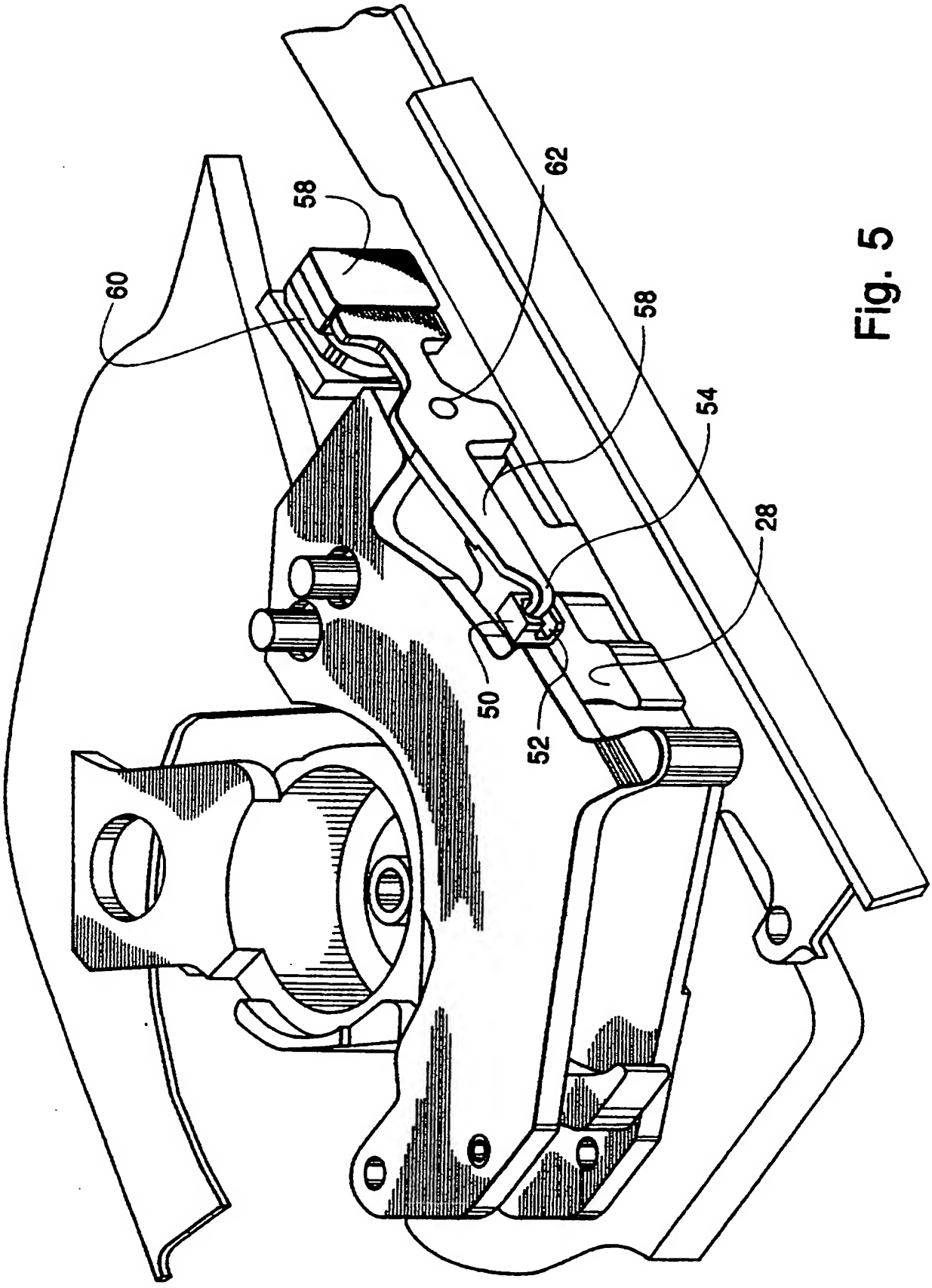

Fig. 5

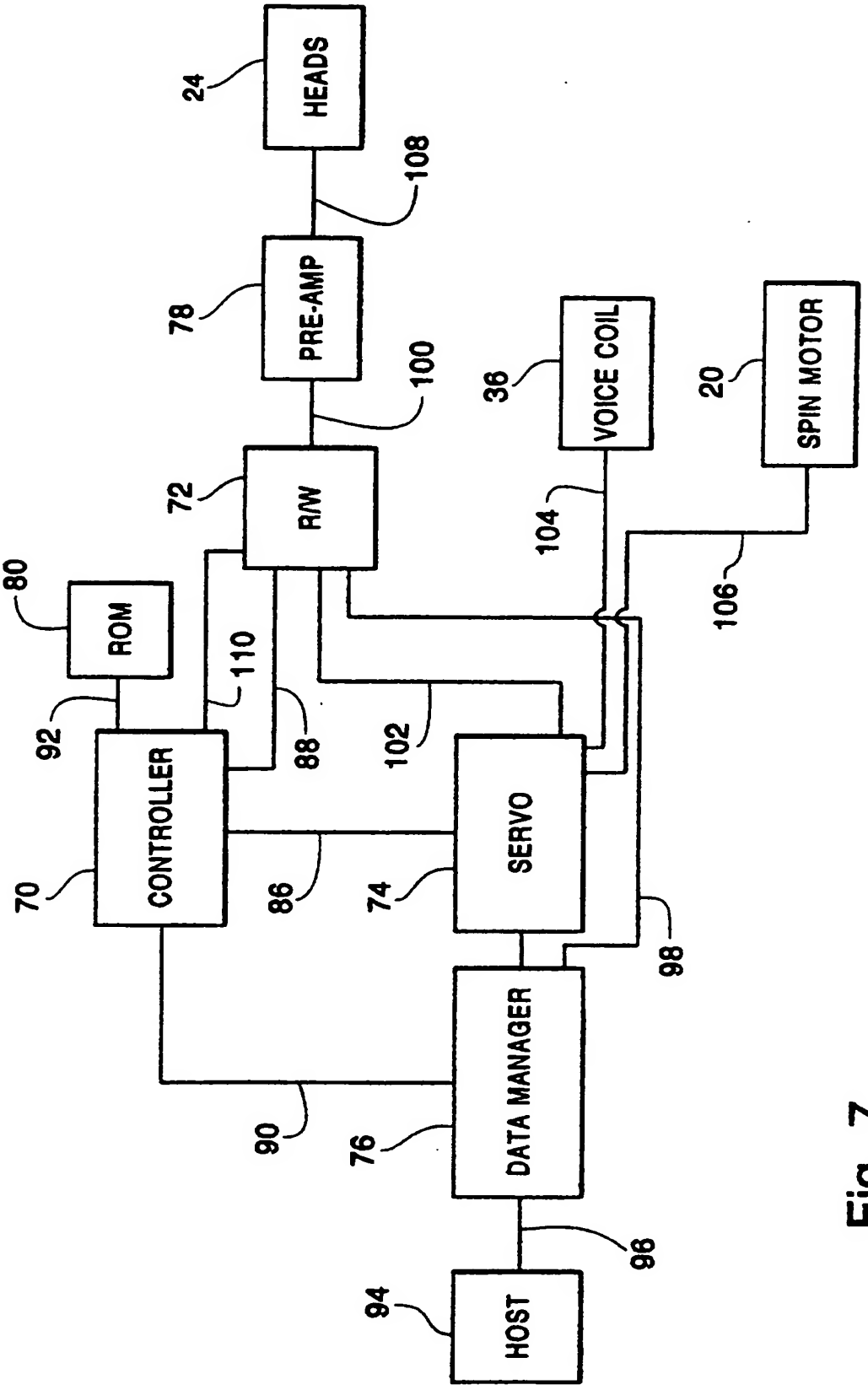
HEADS
24
108
PRE-AMP
78
100
R/W
72
VOICE COIL
36
SPIN MOTOR
20
104
106
ROM
80
110
92
88
102
CONTROLLER
70
86
SERVO
74
98
DATA MANAGER
90
76
96
HOST
94

Fig. 7

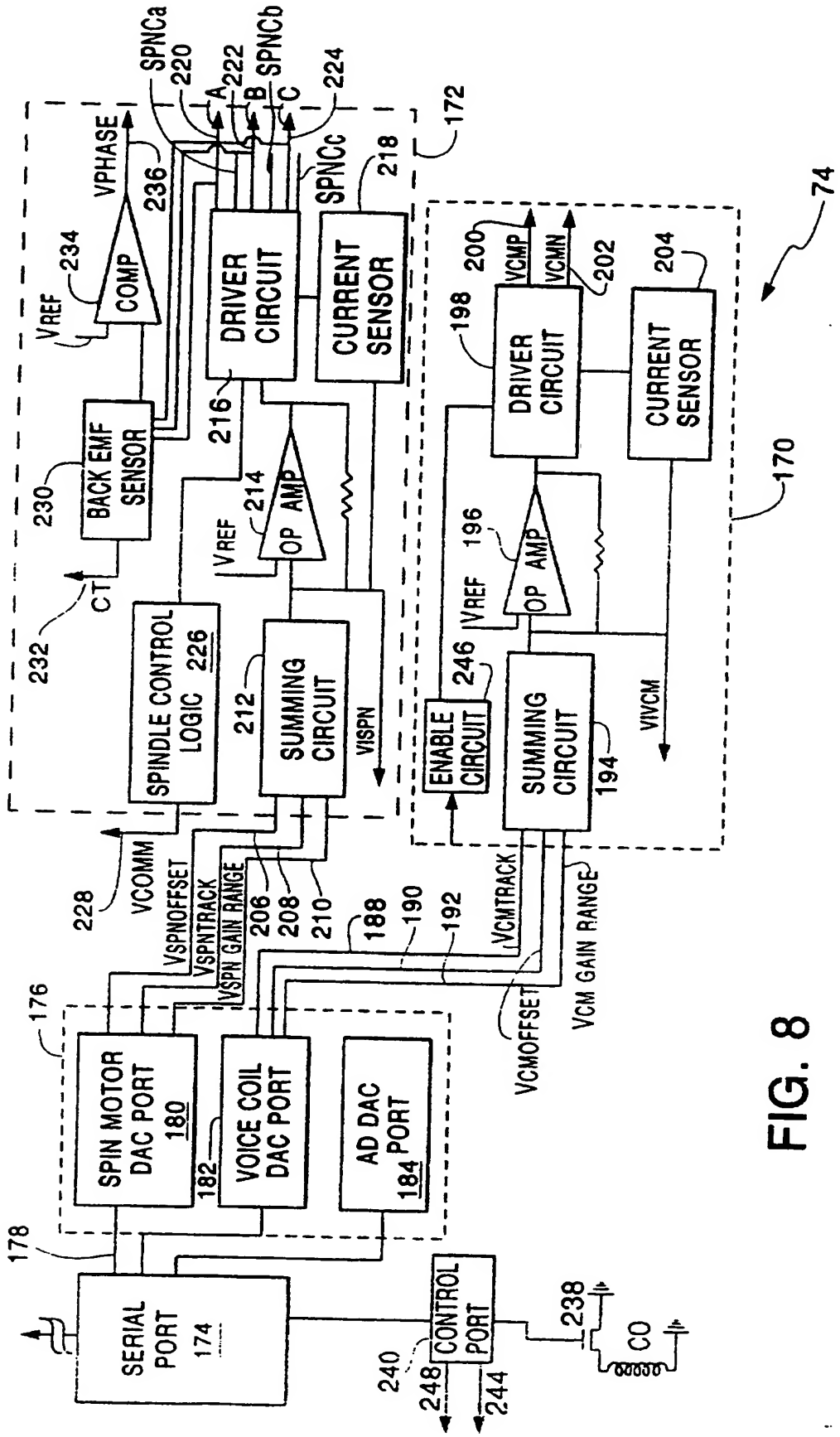
SPNCa
220
A
222
B
SPNCb
C
224
172
VPHASE
236
SPNCc
218
74
234
VREF
COMP
DRIVER CIRCUIT
CURRENT SENSOR
200
VCMP
VCMN
202
204
198
DRIVER CIRCUIT
CURRENT SENSOR
230
BACK EMF SENSOR
216
214
OP AMP
VREF
196
OP AMP
170
232
CT
SPINDLE CONTROL LOGIC 226
212
SUMMING CIRCUIT
VISPN
ENABLE CIRCUIT
246
SUMMING CIRCUIT
194
VIVCM
228
VCOMM
VSPNOFFSET
VSPNTRACK
VSPN GAIN RANGE
206
208
210
188
190
192
VCMTRACK
VCM GAIN RANGE
176
SPIN MOTOR DAC PORT 180
182
VOICE COIL DAC PORT
AD DAC PORT 184
VCMOFFSET
178
SERIAL PORT 174
CONTROL PORT
238
CO
240
248
244

FIG. 8

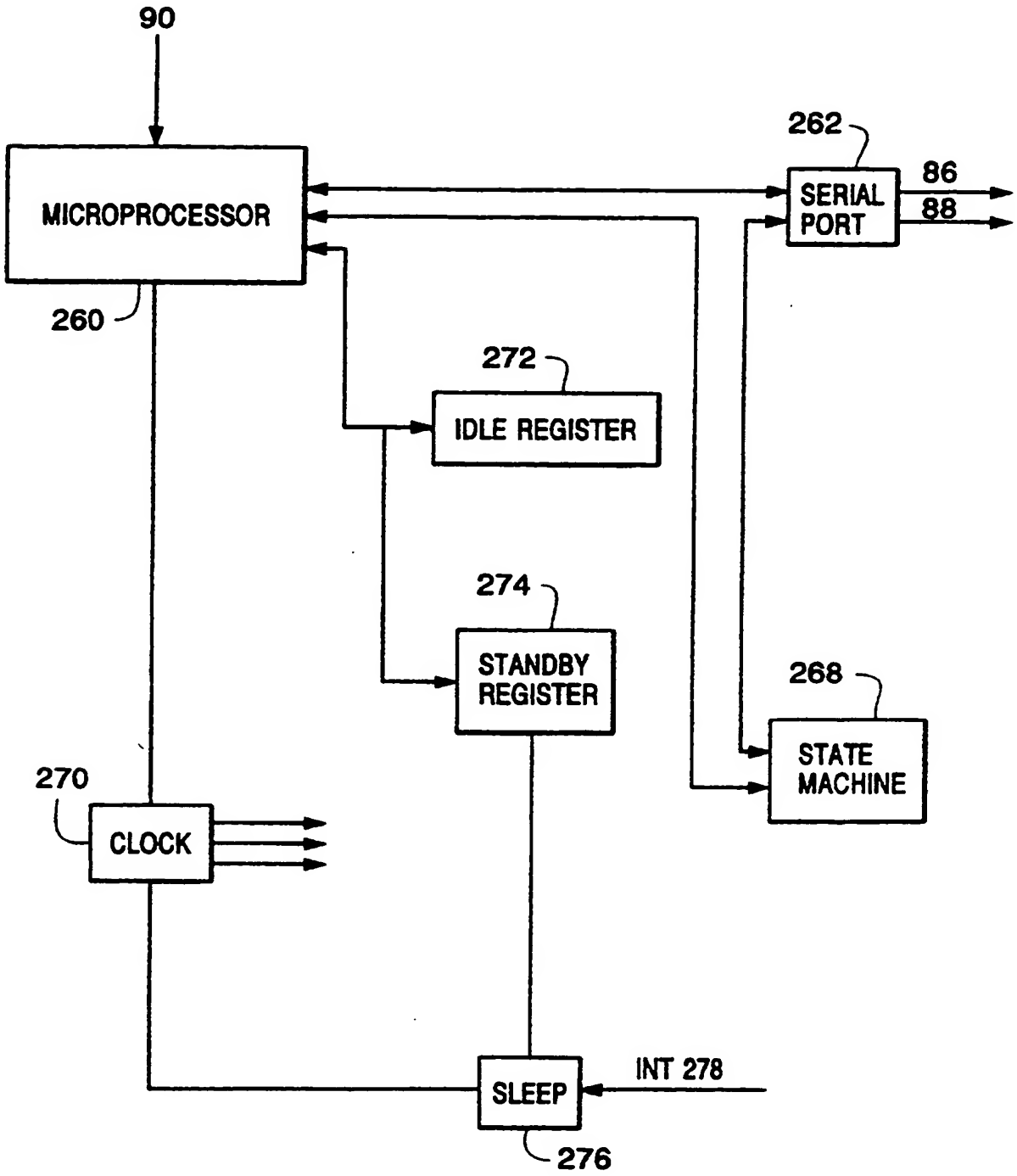
90
MICROPROCESSOR
260
262
SERIAL PORT
86
88
272
IDLE REGISTER
274
STANDBY REGISTER
268
STATE MACHINE
270
CLOCK
SLEEP
INT 278
276

Fig. 9

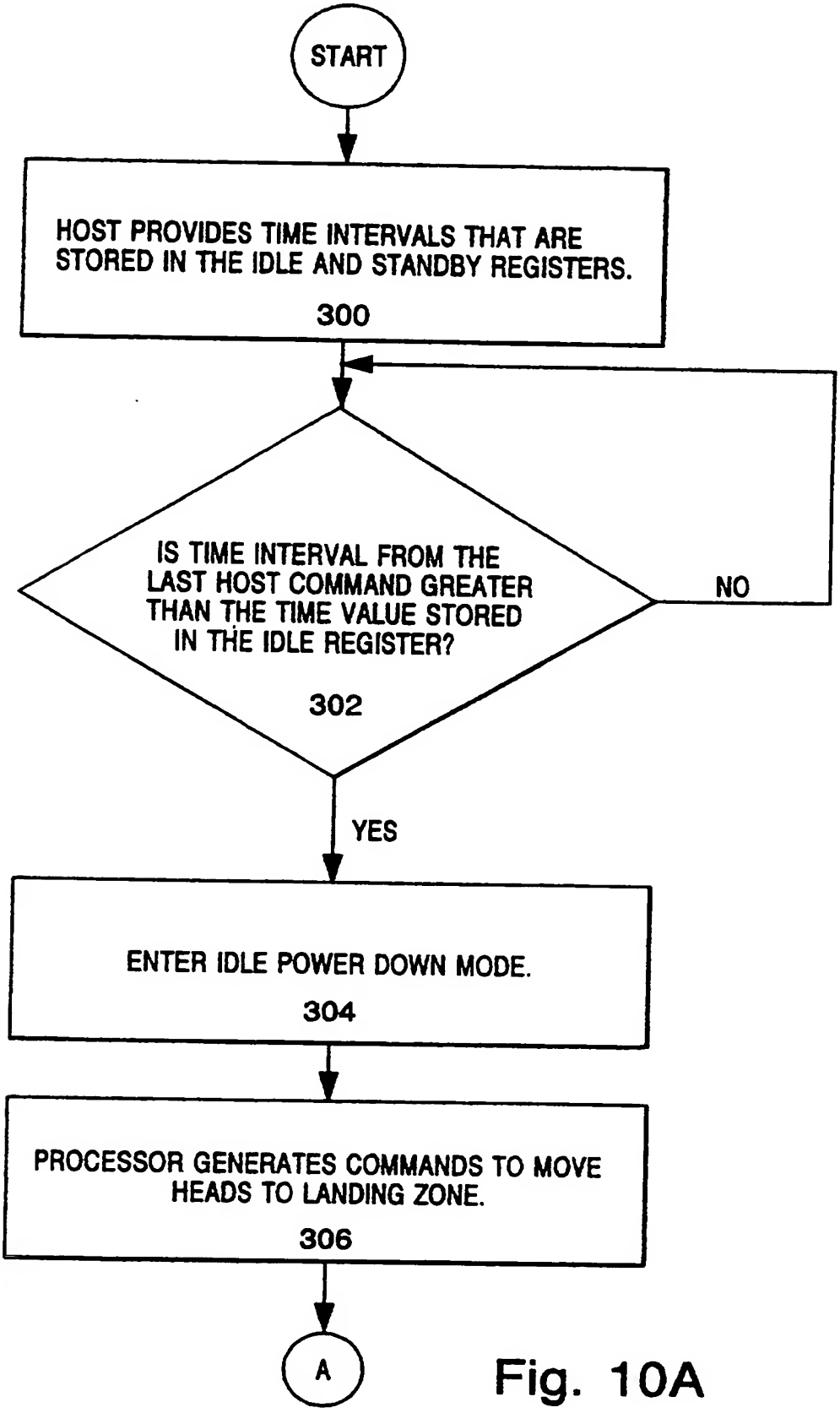
START
HOST PROVIDES TIME INTERVALS THAT ARE STORED IN THE IDLE AND STANDBY REGISTERS.
300
IS TIME INTERVAL FROM THE LAST HOST COMMAND GREATER THAN THE TIME VALUE STORED IN THE IDLE REGISTER?
302
NO
YES
ENTER IDLE POWER DOWN MODE.
304
PROCESSOR GENERATES COMMANDS TO MOVE HEADS TO LANDING ZONE.
306
A

Fig. 10A

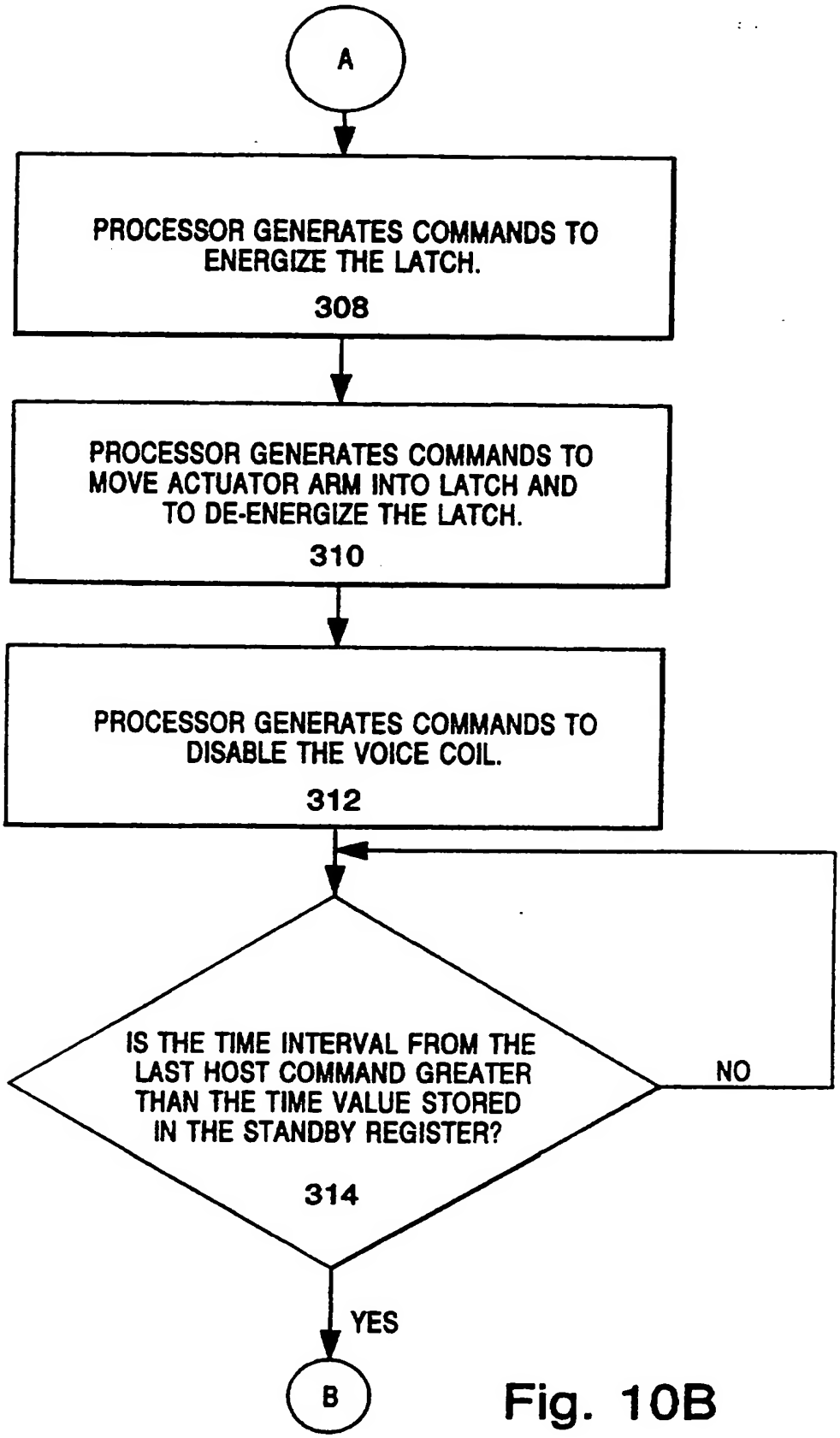
A
PROCESSOR GENERATES COMMANDS TO ENERGIZE THE LATCH.
308
PROCESSOR GENERATES COMMANDS TO MOVE ACTUATOR ARM INTO LATCH AND TO DE-ENERGIZE THE LATCH.
310
PROCESSOR GENERATES COMMANDS TO DISABLE THE VOICE COIL.
312
IS THE TIME INTERVAL FROM THE LAST HOST COMMAND GREATER THAN THE TIME VALUE STORED IN THE STANDBY REGISTER?
314
NO
YES
B

Fig. 10B

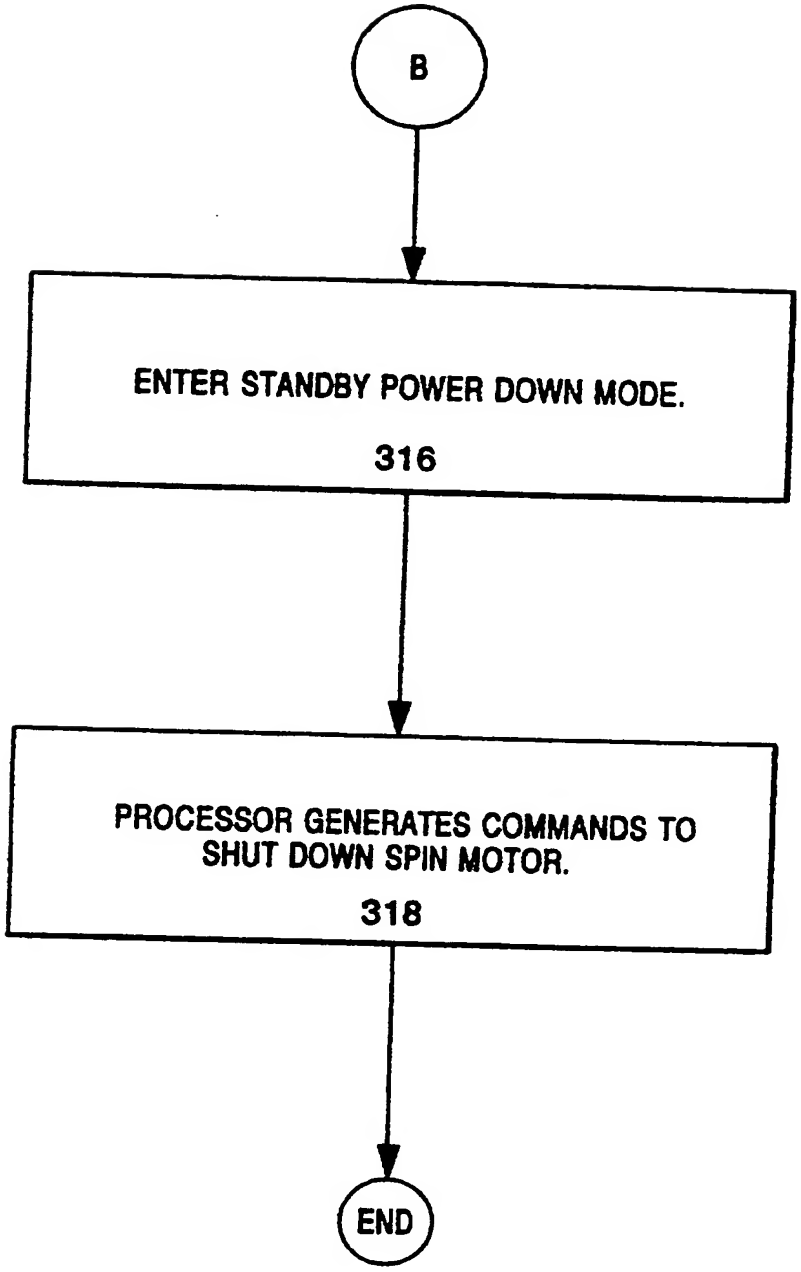
B
ENTER STANDBY POWER DOWN MODE.
316
PROCESSOR GENERATES COMMANDS TO SHUT DOWN SPIN MOTOR.
318
END

Fig. 10C

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US95/12954

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :G11B 5/05, 21/02, 5/596, 5/54
US CL : 360/69, 75, 77.02, 105
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 360/69, 75, 77.02, 105

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X/Y	US, A, 5,216,662 (STEFANSKY ET AL.) 01 June 1993, abstract, col. 5 lines 16-17 and 48-52 and col. 15 lines 29-31.	1 and 17 / 2-16, and 18-23
Y	US, A, 4,933,785 (MOREHOUSE ET AL.) 12 June 1990, abstract, col.4 line 61 - col. 5 line 29, col. 5 line 52, and col. 8 lines 36-44.	2-16 and 18-23

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14 DECEMBER 1995	28 DEC 1995

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Form PCT/ISA/210 (second sheet)(July 1992)*